23. (Amended) A memory circuit, as in Claim 22, wherein the control logic [receives] is adapted to receive an external mode select signal for selecting the burst mode or the pipelined mode and for determining the selected mode control signal.

32. (Amended) A memory circuit, as in Claim 26 [31], [further comprising an asynchronously-accessible memory array coupled for receiving the first external address] wherein the memory circuit is incorporated in an asynchronously-accessible random access memory.